IN THE CLAIMS:

Please substitute the following claims for the same-numbered claims in the application:

1-54. (Cancelled).

55. (Currently Amended) A device for transporting integrated circuit chips and for testing said integrated circuit chips during said transporting, said ~~transportable integrated circuit chip test~~ device comprising:

an in-transit box adapted to transport said integrated circuit chips;

a ~~transportable~~ plurality of test boxes mounted in said in-transit box ~~adapted to surround integrated circuit chips during transportation of said integrated circuit chips~~;

a plurality of test boards mounted in each one of said test boxes and adapted to test said integrated circuit chips during said transporting of said integrated circuit chips ~~while in transit~~; and

a ~~portable~~ power supply in each of said test boxes, connected to each of said test boards, and adapted to supply power to said test boards during said transporting and said testing of said integrated circuit chips ~~while in transit~~,

wherein each of said test boards comprises:

multiple sockets adapted to hold and electrically connect to multiple integrated circuit chips; and

testing circuitry electrically connected to said sockets for testing said multiple integrated circuit chips.

56. (Previously Presented) The device in claim 55, wherein each of said test boards includes visual test failure indicators, such that one of said visual test failure indicators is adjacent each of said sockets.

57. (Currently Amended) The device in claim 55, wherein for each test box said ~~portable~~ power supply comprises a power bus electrically connected between said test boards and one of a battery in said test box and a separate power supply in said in-transit box.

58. (Previously Presented) The device in claim 55, wherein each of said test boards includes a memory adapted to store test results.

59. (Previously Presented) The device in claim 55, wherein each of said test boards includes a known good integrated circuit chip.

60. (Previously Presented) The device in claim 59, wherein each of said test boards includes comparators electrically connected to said sockets.

61. (Previously Presented) The device in claim 60, wherein said testing circuitry is adapted to supply identical test patterns to said integrated circuit chips to be tested and to said known good integrated circuit chip, and

wherein said comparators compare an output generated by said known good integrated circuit chip with outputs generated by said integrated circuit chips to be tested to identify defective integrated circuit chips.

62. (Previously Presented) The device in claim 61, wherein said comparators are in parallel to one another such that all comparisons performed by said comparators are made simultaneously.

63. (Previously Presented) A device for transporting application specific integrated circuit (ASIC) chips and for testing said application specific integrated circuit (ASIC) chips during said transporting ~~transportable integrated circuit chip test device adapted to test application specific integrated circuit (ASIC) chips~~, said device comprising:

an in-transit box adapted to transport ASIC chips;

a ~~transportable~~ plurality of test boxes mounted in said in-transit box ~~adapted to surround integrated circuit chips during transportation of said integrated circuit chips~~;

a plurality of test boards mounted in each one of said test boxes and adapted to test said ~~integrated circuit~~ ASIC chips during said transporting of said ASIC chips ~~while in-transit~~; and

a ~~portable~~ power supply in each of said test boxes, connected to each of said test boards, and adapted to supply power to said test boards during said transporting and said testing of said ASIC chips ~~while in-transit~~,

wherein each of said test boards comprises:

multiple sockets adapted to hold and electrically connect to multiple ASIC chips; and

testing circuitry electrically connected to said sockets for testing said multiple ASIC chips, wherein said testing circuitry includes comparators arranged in parallel and electrically connected to said sockets, such that said testing circuitry tests all of said multiple ASIC chips simultaneously, and

wherein said testing circuitry identifies a defective ASIC chip as one having a different output when compared to outputs of the other ASIC chips, when all of said multiple ASIC chips are supplied with identical inputs.

64. (Currently Amended) The device in claim, 63 wherein all of said multiple ASIC chips have an identical design.

65. (Previously Presented) The device in claim 63, wherein each of said test boards includes visual test failure indicators, such that one of said visual test failure indicators is adjacent each of said sockets.

66. (Currently Amended) The device in claim 63, wherein for each test box said ~~portable~~ power supply comprises a power bus electrically connected between said test boards and one of a battery in said test box and a separate power supply in said in-transit box.

67. (Previously Presented) The device in claim 63, wherein each of said test boards includes a memory adapted to store test results.

68. (Previously Presented) The device in claim 63, wherein each of said test boards includes a known good integrated circuit chip.

69. (Previously Presented) The device in claim 68, wherein all of said comparators are connected to said known good integrated circuit chip such that any ASIC chips that produce an output different than the output produced by said known good integrated circuit chip is identified as a defective ASIC chip.

70. (Previously Presented) The device in claim 63, wherein by comparing whether outputs of all ASIC chips are identical, said testing circuitry does not require a specific proper output that a given input should produce for the specific design of ASIC chip being tested.

71-96 (Cancelled).

97. (Currently Amended) A method for simultaneously transporting and testing integrated circuit chips comprising:

connecting integrated circuit chips to test boards having test circuitry;

mounting said test boards in test boxes having power supplies;

mounting said test boxes in an in-transit box;

transporting said integrated circuit chips in said in-transit box; ~~and~~

testing said integrated circuit chips during said transporting by using said test circuitry; and

supplying power to said integrated circuit chips during said transporting and said testing by using said power supplies.

98. (Cancelled).

99. (Previously Presented) The method in claim 97, further comprising identifying ones of said integrated circuit chips which failed said testing.

100. (Previously Presented) The method in claim 99, wherein said identifying comprises storing results of said testing in a memory.

101. (Previously Presented) The method in claim 99, wherein said identifying comprises displaying a visual indicator of passing or failing chips

102. (Previously Presented) The method in claim 99, wherein said testing includes comparing output signals of said integrated circuit chips with each other.

103. (Previously Presented) The method in claim 97, wherein said testing includes comparing output signals of one integrated circuit chip with output signals of all other integrated circuit chips that have not been identified as defective.

104. (Previously Presented) The method in claim 97, wherein said testing includes comparing output signals of said integrated circuit chips with a golden chip.